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REPORT DOCUMENTATION PAGE

(2)

1a. AD-A200 925 DTIC ELECTE NOV 0 9 1988 D	1b. RESTRICTIVE MARKINGS
2a.	3. DISTRIBUTION/AVAILABILITY OF REPORT: Approved for public release; distribution unlimited.
2b.	
4. PERFORMING ORGANIZATION REPORT NUMBER(S)	5. MONITORING ORGANIZATION REPORT NUMBER(S): ARO 22593.3-EL
6a. NAME OF PERFORMING ORGANIZATION: Cornell university	6b. OFFICE SYMBOL (If applicable)
6c. ADDRESS (City, State, and ZIP Code): School of Electrical Engineering, 425 Phillips Hall, Ithaca, New York 14853	7a. NAME OF MONITORING ORGANIZATION: U. S. Army Research Office
	7b. ADDRESS (City, State, and ZIP Code): P. O. Box 12211, Research Triangle Park, NC 27709-2211
8a. NAME OF FUNDING/SPONSORING ORGANIZATION: U. S. Army Research Office	8b. OFFICE SYMBOL (If applicable)
8c. ADDRESS (City, State, and ZIP Code): P. O. Box 12211, Research Triangle Park, NC 27709-2211	9. PROCUREMENT INSTRUMENT IDENTIFICATION NUMBER: DAAG29-85-K-0213
	10. SOURCE OF FUNDING NUMBERS: PROGRAM ELEMENT NO. / PROJECT NO. / TASK NO. / WORK UNIT ACCESSION NO.

11. TITLE (Include Security Classification)
A Study of $Ga_{0.47}In_{0.53}As/Al_{0.48}In_{0.52}As$ for Very High Frequency Device Applications

12. PERSONAL AUTHOR(S)
Lester F. Eastman and L. F. Palmateer

13a. TYPE OF REPORT	13b. TIME COVERED	14. DATE OF REPORT (Year, Month, Day)	15. PAGE COUNT
FINAL	FROM 9/1/85 TO 5/31/88	10/10/88	13

16. SUPPLEMENTARY NOTATION
The view, opinions and/or findings contained in this report are those of the author(s) and should not be construed as an official Department of the Army position, policy, or decision, unless so designated by other documentation.

17. COSATI CODES		
FIELD	GROUP	SUB-GROUP

18. SUBJECT TERMS (Continue on reverse if necessary and identify by block number)
MODFET, Al,InAs/Ga,InAs/InP, Short Gate, millimeter-wave.

19. ABSTRACT
AlInAs/GaInAs/InP Modulation Doped Field Effect Transistors are investigated for millimeter-wave device applications. AlInAs/GaInAs/InP MODFETs with gate lengths varing from 1.0 μm to 0.1 μm have been successfully fabricated and characterized at DC and microwave frequencies. Measured unity current gain cutoff frequencies between 100-120 GHz and power gain cutoff frequencies between 220-250 GHz are obtained for 0.2 μm gate length MODFETs. Unity current gain cutoff frequencies between 140-150 GHz are measured for 0.1 μm gate length MODFETs. Short gate length effects are studied to understand transport mechanisms in the MODFETs in order to further improve performance. Excess gate current due to hot electron effects are observed in short gate MODFETs. The RF and DC output conductance characteristics are measured and analyzed. New structures including variations in buffer layer design, atomic planar doping profiles, strained layer structures and mismatched structures are investigated.

20. DISTRIBUTION/AVAILABILITY OF ABSTRACT	21. ABSTRACT SECURITY CLASSIFICATION
☐ UNCLASSIFIED/UNLIMITED ☐ SAME AS RPT. ☐ DTIC USERS	Unclassified
22a. NAME OF RESPONSIBLE INDIVIDUAL	22b. TELEPHONE (Include Area Code) / 22c. OFFICE SYMBOL

DD FORM 1473, 84 MAR — 83 APR edition may be used until exhausted. All other editions are obsolete.

SECURITY CLASSIFICATION OF THIS PAGE
UNCLASSIFIED

54

ARO 22593.3-EC

A STUDY OF $Ga_{0.47}In_{0.53}As/Al_{0.48}In_{0.52}As$ FOR VERY HIGH FREQUENCY DEVICE APPLICATIONS

FINAL REPORT

Lester F. Eastman, L.F. Palmateer

September 1, 1985 - May 31,1988

U.S. ARMY RESEARCH OFFICE

DAAG29-85-0213

CORNELL UNIVERSITY

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AlInAs/GaInAs/InP MODFETs have proven superior device performance over the more conventional AlGaAs/GaAs MODFET and have attracted a great deal of attention for low noise high-frequency device applications. The AlInAs/GaInAs material system has the advantages of having large GaInAs/AlInAs heterojunction conduction band discontinuity, ΔE_C=0.5eV, large room temperature mobilities and superior electron transport properties in GaInAs, and large Γ–L energy separation in GaInAs.

Itoh et al (1985) at Cornell, employing a recessed gate technology, demonstrated the first successful fabrication of Enhancement- and Depletion-mode AlInAs/GaInAs/InP MODFETs. The 1.2 μm Gate Length MODFETs were measured at microwave frequencies from 0.5 GHz to 26.5 GHz yielding a unity current gain cutoff frequency (f_T) of 22 GHz, proving an improvement in microwave performance of over the conventional AlGaAs/GaAs MODFET. These results, published by *Palmateer et al* (1987), were the first report of microwave characterization of MODFETs in this material system.

AlInAs/GaInAs/InP MODFET structures with strained and lattice-matched GaInAs channels and double-doped heterojunctions were grown and 1.0 μm gate length MODFETs were fabricated. The doping-thickness product of the AlInAs in the MODFET structures was investigated using Si-doping $1x10^{19}$ cm^{-3} with varying thicknesses of 30Å, 40Å, 50Å and 100Å. High room temperature Hall mobilities, 9,000-11,500 cm^2/V-sec, with Hall sheet densities between 1.3-3.3 $x10^{12}$ cm^{-2} were measured on the single doped structures.

The strained epilayer structures were grown with Indium rich GaInAs channels, ≈55% and ≈64% In. The 1.0 μm gate length MODFETs fabricated on these structures indicated an improvement of ≈5-10% in transconductance and

current densities compared to the lattice matched structures of comparable doping thickness product. The 1.0 μm gate length strained channel MODFETs had extrinsic transconductances (g_m) between 350-388 mS/mm at current densities between 190-200 mA/mm. The double-doped epilayer structures gave room temperature Hall mobilities of 9,000 cm^2/V-sec with Hall sheet densities of 3.5×10^{12} cm^{-2}. The 1.0 μm gate length double-doped MODFETs had g_m=380 mS/mm at 500 mA/mm. In order that the high current densities available in the double-doped structures be considered useful for power device applications a better understanding of the breakdown mechanisms of the Schottky barrier gate and in high field gate to drain region must be investigated.

Obtaining low parasitic resistances is extremely important for high performance low noise devices. Low parasitic resistances should be possible in AlInAs/GaInAs/InP structures due to the high mobilities and the high sheet densities available in GaInAs, which provide a highly conductive GaInAs channel. Ohmic contact studies were performed using varying thicknesses of the ohmic metallization and optimizing the alloy temperatures using the Rapid Thermal Annealing system. The preferred ohmic metallization is Ni(100Å)/Ge(400Å)/Au(800Å)/Ag(200Å)/Au(800Å) rapid thermal annealed for 10 seconds at 350°C which gave the lowest TLM contact resistances of 0.1 Ω-mm. Ohmic contact formation is complicated in the AlInAs/GaInAs/InP device structure due to the necessity of the undoped AlInAs layer under the recessed gate required for the formation of a Schottky barrier on AlInAs. The region of undoped material is not desirable for the formation of ohmic contacts. Non-alloyed ohmic contacts were investigated where doping spikes were used in the AlInAs top epilayer in order provide the possibility of direct ohmic contact formation to the epilayer through tunneling assisted ohmic contacts. The

contacts required an alloy cycle in order to achieve contact resistances below 0.4 Ω-mm. Further studies are necessary to determine the required epilayer design for the non-alloyed contacts.

A planarized process has been investigated where a Boron implant is used for mesa isolation instead of the wet chemical mesa etch. The Boron was implanted with a two stage process using a dose of 2.0 x10 ^{13} cm^{-2} Boron at 40 KeV and 3.0 x 10^{13} cm^{-2} Boron at 60 KeV. The Boron implanted devices were completely isolated and had performance comparable to the etched mesa devices. The use of a planarized process may become important for device applications in order to eliminate the region where the gate metallization comes in contact with the GaInAs channel in the etched mesa devices. In the etched mesa devices the gate metallization comes in contact with the GaInAs channel at the mesa plateau and may cause a degradation of device performance.

AlInAs/GaInAs/InP 0.2μm Gate Length T-gate MODFETs have been fabricated and measured on wafer over the frequency range from 0.5 GHz to 26.5 GHz using the CASCADE MICROTECH PROBER and the HP8510 network analyzer. The epilayer MODFET structures are MBE grown lattice-matched to InP substrates. The structure is as follows:

1. GaInAs capping layer: Si doped 1x10^{19}cm^{-3} 200Å
2. AlInAs: Si doped 1x10^{19}cm^{-3} 30Å
3. AlInAs undoped: 200Å
4. AlInAs: Si doped 1x10^{19}cm^{-3} 100Å
5. AlInAs undoped spacer: 20Å
6. GaInAs undoped channel: 500Å
7. AlInAs 40Å/GaInAs 10Å superlattice buffer: 5000Å
8. InP Semi-Insulating Substrate

The 0.2 μm gate length MODFETs have a measured extrinsic g_m=665mS/mm at V_d = 2.0 V, V_g = +0.3V and I_d = 235mA/mm. The measured S-parameters on 0.2 μm gate length T-gate MODFETs yield unity current gain cutoff frequencies, f_T's, between 100-120 GHz and f_{max} between 230-250 GHz. A low value of feedback capacitance was measured on the MODFETs which is important to achieve high f_{max}. Further measurements and analysis are required to better understand and optimize the factors contributing to the low feedback capacitance in order that the best performance can be achieved. The MODFETs maintain high measured f_T's down to low drain currents, which is particularly attractive for low-noise device applications. Typically in the short gate length AlInAs/GaInAs MODFETs the maximum drain-source voltage which can be applied is 2.0V. Typically, the measured f_T and f_{max} of these devices continue to increase with drain-source voltage and do not reach their maximums before the devices are seen to breakdown. The nature of the breakdown mechanisms in AlInAs/GaInAs/InP MODFETs are not understood. Weak avalanching in the gate-drain region or in the GainAs channel or Schottky barrier breakdown may be effecting the breakdown. It is important that future studies concentrate on understanding the breakdown mechanisms in the devices in order to achieve the maximum obtainable performance. The breakdown mechanisms can be further understood by noise measurements and analysis on the MODFETs.

Effects influencing the device performance, especially important at short gate lengths, have been studied on the 0.2μm gate length AlInAs/GaInAs MODFETs:

1.) Excess gate current due to hot electron effects and

2.) the disparity in the DC and RF output conductance.

Excess Gate current due to hot electron effects was observed in 0.2μm Gate

Length MODFETs with measured f_T's of 100 GHz. These results were reported at the International Symposium on GaAs and Related Compounds, Atlanta, Georgia, 1988. The dependence of gate current on source drain voltage in the DC I-V characteristics of the Enhancement-mode MODFETs is evidence of hot electron real space transfer over the large heterojunction barrier, ΔE_C =0.5eV, where some of these hot electrons are then collected as gate current. The resulting negative diode impedance, observed for the first time in the RF data, is a direct measurement at RF frequencies of hot electron effects, and indicates the mechanism is a high-speed phenomena. The existence of hot electrons due to real space transfer effects may be a limiting factor affecting the cutoff frequency and device performance, especially at short gate lengths and requires further study.

The output conductance, g_{out}, is an important device parameter effecting the power gain, f_{max}, of the MODFET. We report DC and RF and measurements that indicate that the observed "kink effect" in AlInAs/GaInAs/InP MODFETs, characterized by a large increase in output conductance in the DC I-V characteristics, is a DC mechanism, not present at RF frequencies. The disparity between the DC and RF g_{out} measured on 0.2μm gate length MODFETs is seen to be as high as a factor of 5: the DC g_{out} is 160 mS/mm compared to the RF (26GHz) g_{out} = 30 mS/mm. This frequency dispersion may be related to trapping mechanisms in either the top AlInAs or the AlInAs buffer.

In order to study the effects of the buffer layer on the device performance and the "kink effect", a MODFET epilayer was grown identical in structure to that described above except the buffer layer was grown with low arsenic over-pressure in the AlInAs. The kink effect was not observed in the I-V characteristics of the 0.2μm Gate Length MODFETs. The measured f_T of the 0.2μm Gate Length

MODFETs is between 100-120 GHz and the measured f_{max} between 230-250 GHz. The measured DC and RF output conductances were identical: 30-50 mS/mm. These results indicated that the growth and design of the epilayer structure, especially the AlInAs, is an important parameter effecting device performance. Further study is required to understand the the "kink effect" which may be related to trapping and breakdown mechanisms in the MODFETs.

The MODFET structure described above with the buffer layer grown at low arsenic over-pressure, was used to fabricate 0.1 μm gate length devices using the JEOL Electron Beam Lithography machine. Even though process related problems caused a high source resistance, 1.4 Ω-mm, which lowers the measured f_T , an f_T of 150 GHz was measured on the devices. Clearly, these results are incentive to pursue ultra-short gate length AlInAs /GaInAs MODFETs.

As shorter gate length MODFETs are fabricated and and higher average electron velocities. are achieved, the need for improvements in electron confinement become increasingly more important. The observation of the excess gate current due to hot electron effects observed in the 0.2 μm gate length devices is evidence that the real space transfer of electrons out of the GaInAs channel is occurring and may be an important factor limiting the performance of the devices. In order to investigate the effects of the conduction band discontinuity on device performance, an $Al_{0.70}In_{0.30}As/Ga_{0.70}In_{0.30}As$ lattice mismatched on a GaAs substrate and a lattice matched $Al_{0.48}In_{0.52}As/Ga_{0.47}In_{0.53}$ on an InP substrate were grown for comparison. The compositions: $Al_{0.70}In_{0.30}As/Ga_{0.70}In_{0.30}As$ were chosen as to maximize the available heterojunction conduction band discontinuity in this system before the indirect crossover point. MODFETs with 0.2 μm gate lengths were fabricated on both epilayer structures. The high Al mole fraction, x = 0.70, in the

top AlInAs layer of the mismatched structure succeeded in improving the reverse bias Schottky gate leakage current in the MODFET: the room temperature reverse leakage current of the mismatched MODFET was reduced by a factor of 150 compared to the lattice matched MODFET at comparable bais conditions. The DC and microwave performance of the two structures were comparable, but both structures had lower g_m and measured f_T's than expected compared to lattice-matched structures previously fabricated and characterized. The reasons for this are currently being investigated. Both structures used atomic planar doping in the AlInAs, which is a novel growth technique in this material system, and not well characterized. The non-optimized atomic planar doping profiles may account for the lowered performance. Most notable in the $Al_{0.70}In_{0.30}As/Ga_{0.70}In_{0.30}As/GaAs$ lattice mismatched MODFET is the reduction of gate leakage current and the fact that it had performance comparable to the lattice matched structure. The reduction of gate leakage current should provide a significant improvement in overall device performance.

Atomic planar doped epilayer designs have been shown to improve the device performance in pseudomorphic AlGaAs/GaInAs/GaAs MODFETs. The improvements in efficient charge control and device performance using atomic planar doping techniques in those structures is incentive to pursue similar structures in AlInAs/GaInAs/InP MODFETs. A series of atomic planar doped AlInAs/GaInAs MODFET structures with varying spacer thicknesses and doping densities have been grown and are currently been processed.

Optimized device structures should greatly improve the performance of AlInAs/GaInAs/InP MODFETs. Efficient epilayer design reduces the possibility of parallel conduction in the high band-gap material which severely degrades performance. A device simulator program, developed by Mark Foisy at Cornell, which self-consistently solves the coupled Poisson and Schrödinger equations

has proven extremely valuable in predicting the device performance based on epilayer design in the AlGaAs/GaInAs/GaAs material system. The program is currently being modified to include the AlInAs/GaInAs/InP material system and should prove valuable in the design and understanding of optimized device structures. With the aid of the device simulator program, the effects of the epilayer design parameters on device performance, such as the doping thickness product, atomic planar doping profiles, spacer layer thicknesses and channel thicknesses, can be modeled and then tested experimentally and compared. Optimized device structures will also help to standardize the epilayer design which will facilitate epilayer design dependent variables such as ohmic contact formation

In conclusion, short gate length AlInAs/GaInAs/InP MODFETs have been successfully fabricated and have excellent microwave device performance, but can be considered far from optimized. The existence of excess gate leakage current due to hot electron effects, shown here to be present in short gate length devices, is incentive to pursue variations in band-gap engineering in this material system in order to better confine the electrons in the channel. Preliminary results shown lattice-mismatched designs, as well as achieving a larger conduction band discontinuity, succeeded in improving the Schottky gate barrier height to AlInAs and reducing the gate leakage current. Improvements in the Schottky barrier gate are important and necessary for the AlInAs/GaInAs/InP MODFETs to be considered good candidates for power applications and low-noise device applications. Initial studies on 1.0 μm gate length strained layer channel AlInAs/GaInAs/InP MODFETs indicate higher performance can be obtained in strained GaInAs channels compared to the lattice-matched condition. In order to evaluate the use of strained GaInAs

channels on high frequency device performance, short gate length MODFETs must be fabricated. The results obtained concerning the "kink effect" in AlInAs/GaInAs/InP MODFETs show that further studies in the materials growth and analysis is required, especially involving trapping centers in the AlInAs and buffer layer design, which may also help to provide a better understanding of the breakdown mechanisms in the MODFET.

We acknowledge Bill Schaff, Torsten Griem and April Brown for MBE growth, Paul Tasker for assistance in microwave measurements and analysis, and Loi Nguyen and Allen Lepore for mask set design and Rich Tiberio for the 0.1μm gate level definition using the JEOL.

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September 1, 1985 - September 30, 1988

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